Test Report
On
Engineering Model Detector (NUV Channel)
Of
UVIT Payload

Version 0.2

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1. Introduction

UVIT is one of the five payloads on ASTROSAT, first Indian Multi wavelength Astronomical satellite. UVIT aims to image selected parts of the sky in three distinct spectral regions (FUV, NUV and VIS) using two identical telescopes. Before launching the satellite, it is mandatory to test the satellite on the ground itself with all its subsystems and payloads. So, it is also mandatory for us to test the UVIT payload individually, scientifically and technically at IIA before its integration with the spacecraft.

The scientific and technical tests are being done on Engineering Model, to find any error in payload subsystem design, so that error can be corrected in Flight Model Design of the payload for the accuracy and objective fulfillment of the payload. Keeping all these concerns in mind UVIT Engineering Model Detector (NUV Channel) being tested at MGMK Lab, IIA Hosakote.

2. Arrival of UVIT EM Detector System (UVIT EM DS) at IIA

UVIT EM DS arrived in MGMK lab IIA at hosakote on 29th Dec 2008 in evening. All the boxes [Total 8 Boxes; {CPU, HVU, EGSE, EU, Cables, Transformer, Printer, Gasket}] were unloaded and snaps were taken while after unloading. After unloading it was found that Shock Watch Monitor on CPU and HVU boxes was RED, rest other boxes' shock watch monitors were correct. The packing boxes of EU and CPU were having cuts on them. All the boxes were kept in 3Lakh Clean room after cleaning with vacuum cleaner.

Figure 2. 1 HVU Box with RED Shock Watch Monitor

Figure 2. 2 CPU Box with RED Shock Watch Monitor

Figure 2. 3 Damaged CPU Packing Box

3. Opening and Cleaning of UVIT EM DS Boxes

One by One opening of boxes started on 12th Jan 09 in afternoon, in the presence of Mr. Joe Postma in clean area of 1Lakh class. While opening of the boxes snaps were taken at each step to maintain the log of it.

3.1 CPU

First CPU box opened in 1Lakh class on Optical table and found that inside there was one more PVC box present and the shock watch monitor of that PVC box was Un-Triggered. The PVC box was cleaned and moved to class 10K optical table for further opening. PVC box opened and CPU was packed in Vac sealed ESD bag. The ESD bag cleaned from outside with IPA and CPU moved to Class 1K clean area for storing it in desicator.

3.2 HVU

HVU box was opened on optical in 1Lakh clean room. HVU outer box was of metal not of card board as of CPU. Inside Box of HVU was also of metal and the shock watch monitor of inner box was Un-Triggered. Inner box was cleaned with IPA and moved to Class 10K area for further opening. HVU unit was packed in an ESD bag and mounted on a metal plate to the inner box with the shock absorbers in between. HVU box was moved to class 1K for storing it in desicator.

3.3 EU

EU box was also opened in 1Lakh class on Optical table and found that inside there was one more PVC box present and the shock watch monitor of that PVC box was Un-Triggered. The PVC box was cleaned and moved to class 10K optical table for further opening. PVC box opened and EU was packed in Vac sealed ESD bag. The ESD bag cleaned from outside with IPA and EU moved to Class 1K clean area for storing it in desicator.

3.4 EGSE

After this EGSE was cleaned thoroughly in class 1lakh area. The base of EGSE rack is of wood and open wooden part of the EGSE was sealed with the aluminum tape to maintain the cleanliness. EGSE kept in class 1Lakh area to check its own operation before shifting it to class 10K.

Following the same procedure box of cables also opened; each and every cable cleaned with IPA to remove any dust sitting on them. Cables were checked for the continuity and cross continuity to ensure that, there is no damage during transport.

3.5 Transformer

Transformer [240V to 120V] box was opened and cleaned thoroughly. To check, whether it is OK or not, it was powered ON (OFF load) for testing, the LAB MCB trigerred. Transformer didn't turn ON. Cover of transformer opened and was found that the transformer was damaged and cannot be used. To start the test, a transformer was procured from the local market.

In parallel a good 1.5 KVA, 240 to 120 V isolation transformer was ordered from IIA for this. Now the ordered isolation transformer has been installed with EGSE system after checking it.
Printer box opened, cleaned and shifted to BMS (Building Management Systems) for installation. It is working fine.
Box opening finished on 13th Jan 09 (forenoon).

4. First Time Power on UVIT EM DS in IIA

Initially EGSE alone was powered ON to check it correctness (15th Jan 09). It worked fine and was ready to connect it with UVIT EM DS. After that it is moved to class 10K to start testing.
After that EU (packed in ESD bag) was brought from desicator (class 1K) to class 10K optical table (16th Jan 09). ESD bag opened and EU unit cleaned thoroughly with IPA. EU kept on a Stainless Steel movable cart in class 10K near the Small Vacuum Tank (SVAC-1).
Now EU connected with EGSE as per the procedure mentioned in EGSE manual and guidelines of Mr J.Postma.
Now EU alone connected with EGSE. EU powered ON through commands from EGSE and checked thoroughly to ensure its correctness before connecting it with CPU and HVU.
First HVU was brought from class 1K desicator and un-mounted from its box and mounted on a platform, which will be mounted on SVAC-1. HVU body was cleaned with IPA.
After this CPU (packed in ESD bag) was brought from class 1K desicator to class 10K optical table. ESD bag opened and CPU window was covered with a metal plate. CPU body cleaned with IPA.
After cleaning CPU was mounted on a platform, so that CPU & HVU can be mounted on SVAC-1. This activity was done on optical table in Class 10K. Then high voltage cable between CPU and HVU was connected.
First only CPU was connected with EU not HVU, and EGSE, EU and CPU powered ON and the setup was thoroughly checked. It worked properly. The whole system brought to shut down. After this test, HVU connected with EU.
The whole system [EGSE-EU-CPU & HVU] powered ON and dark current reading has taken from CPU, with high voltages is ON. This test also performed on Optical table in Class 10K.

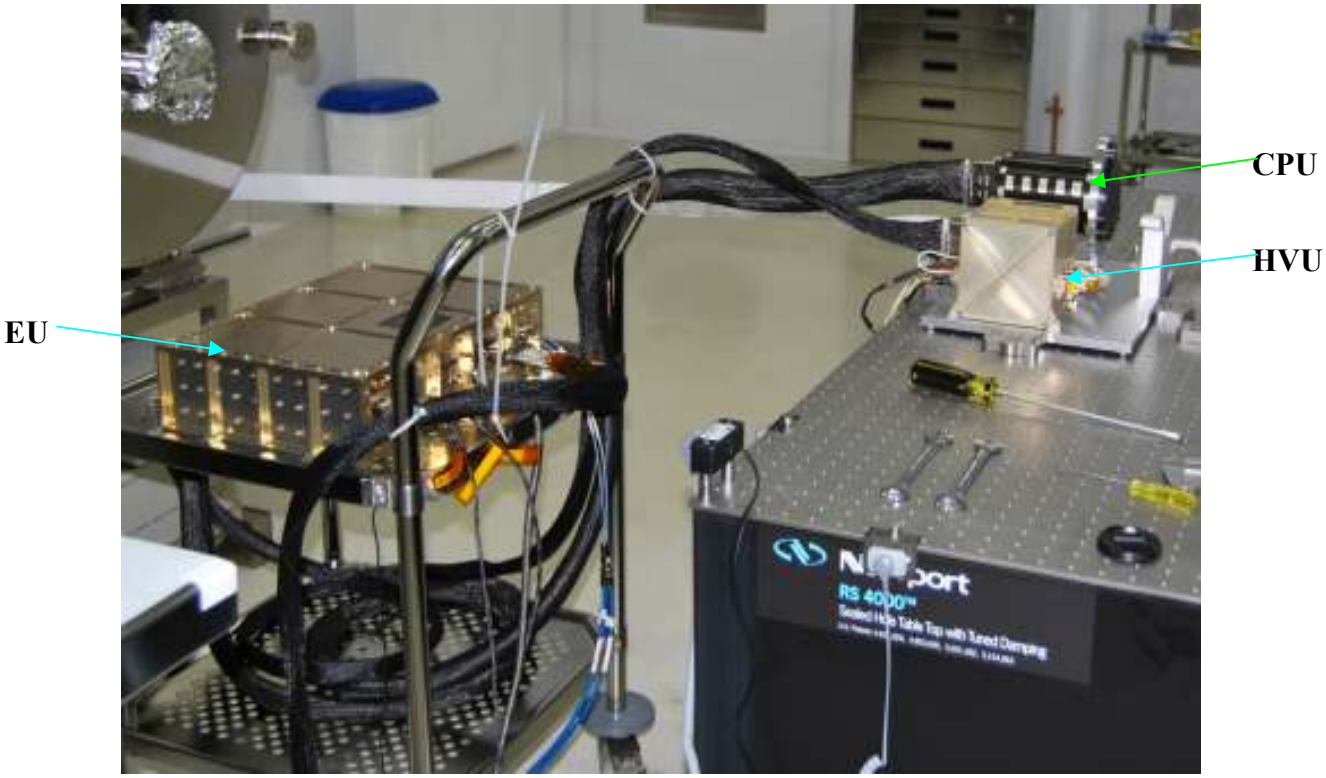

Figure 4. 1 EU-CPU and HVU connected and Placed on Optical Table [Class 10k]

5. Tests Done on UVIT EM DS

On 19th Jan 09, CPU and HVU fixed on same platform mounted on SVAC-1 and again dark current image was taken to check any light leakage in the SVAC-1. It was found that the vacuum gauge was giving some light leakage, so it was decided that vacuum gauge must be OFF while doing imaging with UVIT EM DS.

After confirming that there is no light leakage, UV source put ON and imaging done in both, integration and photon counting mode with UVIT EM DS.

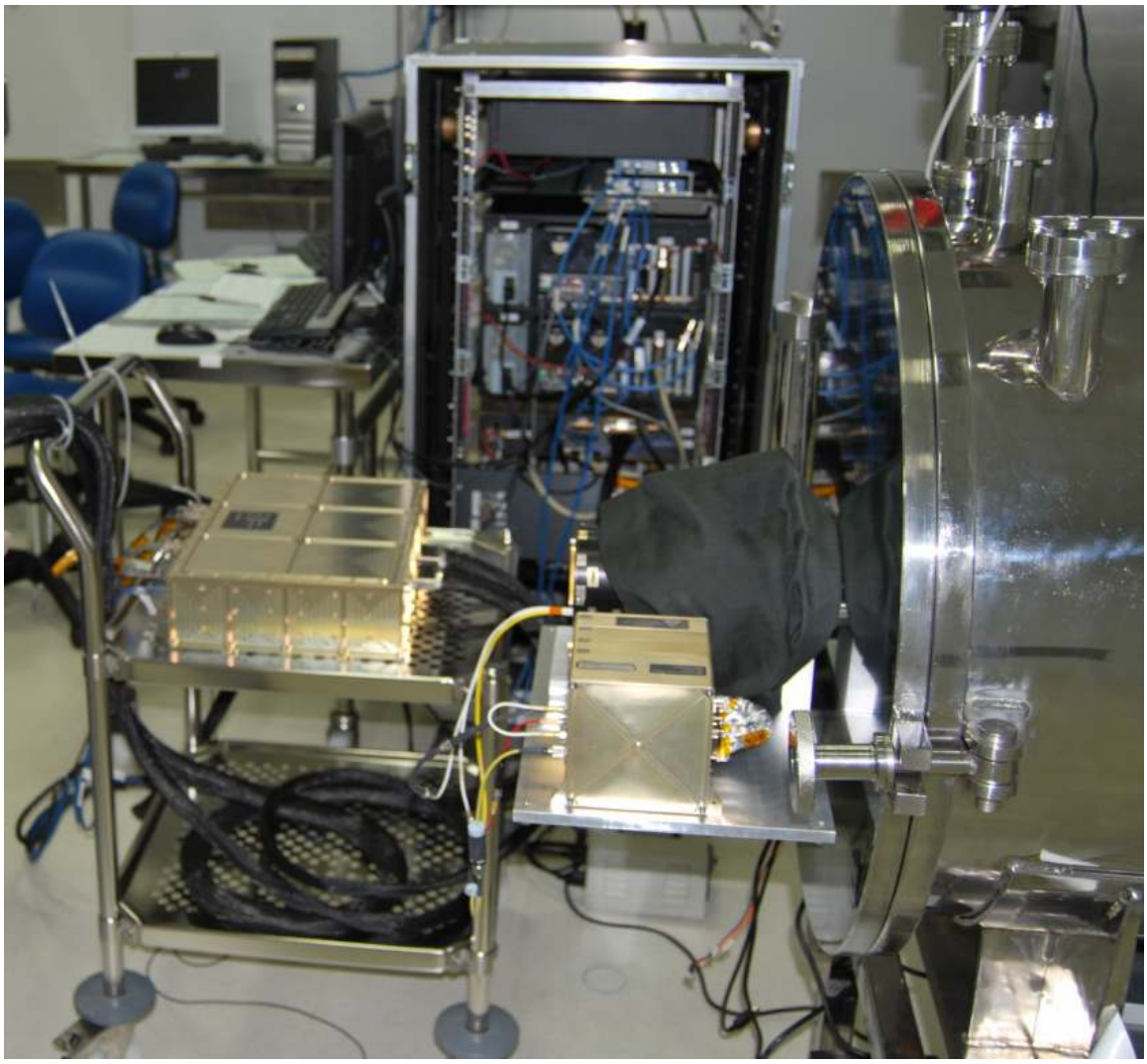

Figure 5. 1 UVIT EM DS Test Setup in MGKM Lab (Class 10K) CREST, IIA

5.1 Following tests were done on UVIT EM DS when Mr. Joe Postma was present:

1) Dark current.
2) Verification of Bright Object Detected (BOD) alarm.
3) Uniformity of the detector window.
4) Wavelength scan from 160 nm to 360 nm.
5) Performance of CPU and HVU with different cable lengths [3.2 mt and 1 mt] between CPU and EU.
6) Imaging done in Integration and Photon Counting mode [3C, 3S and 5S] with pin hole mask.
7) Imaging done with varying the slit width.
8) Hands on training taken on CCDLAB software developed by Joe.

During tests it was observed, CPU window was little dirty and because of that results of imaging was not perfect. Mr. Joe cleaned the CPU window with spectroscopy grade IPA. After cleaning also, CPU window was inspected with black light to see any dust is there or not.
Imaging was done after cleaning and the results were satisfied.

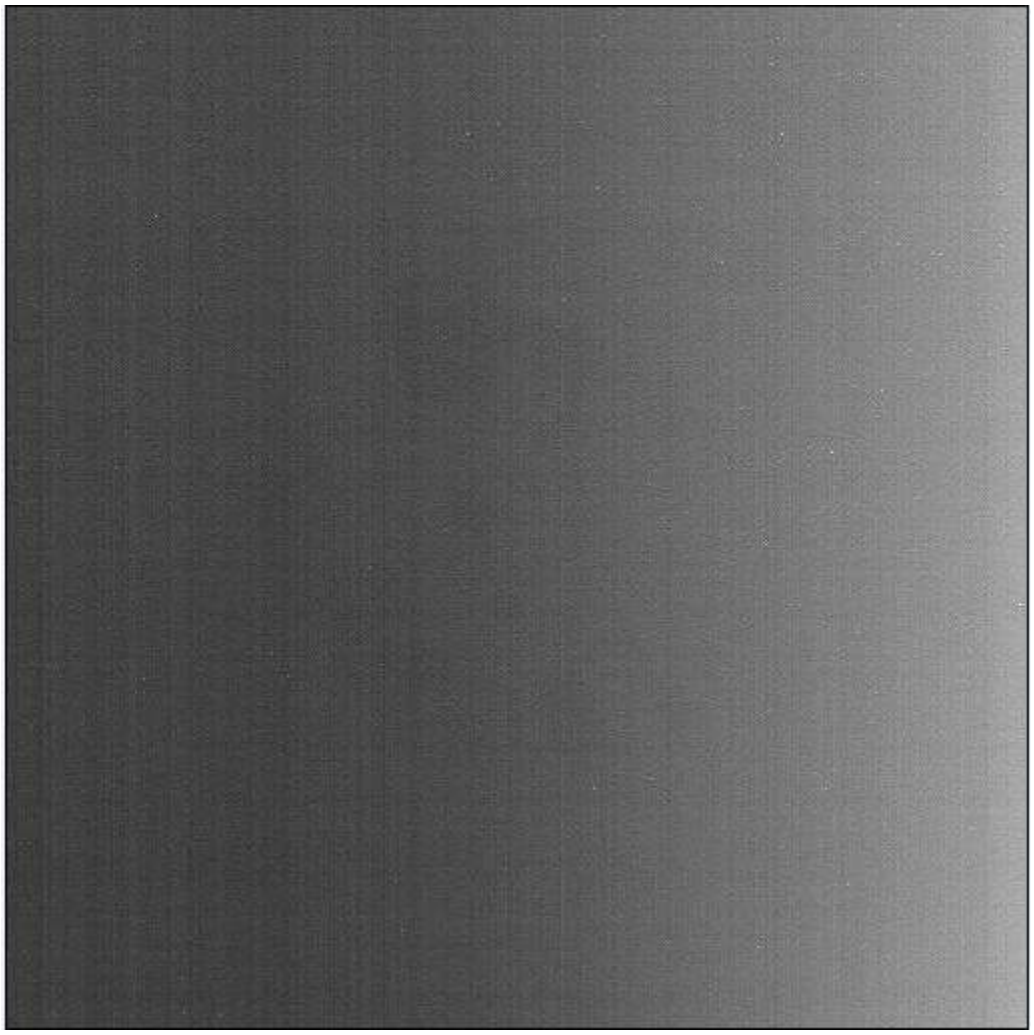

Figure 5. 2 Dark Current Output of CPU [Single Frame, 400th Frame]

Figure 5. 3 Image in Integration Mode [Single Frame, 400th Frame, Source ON]

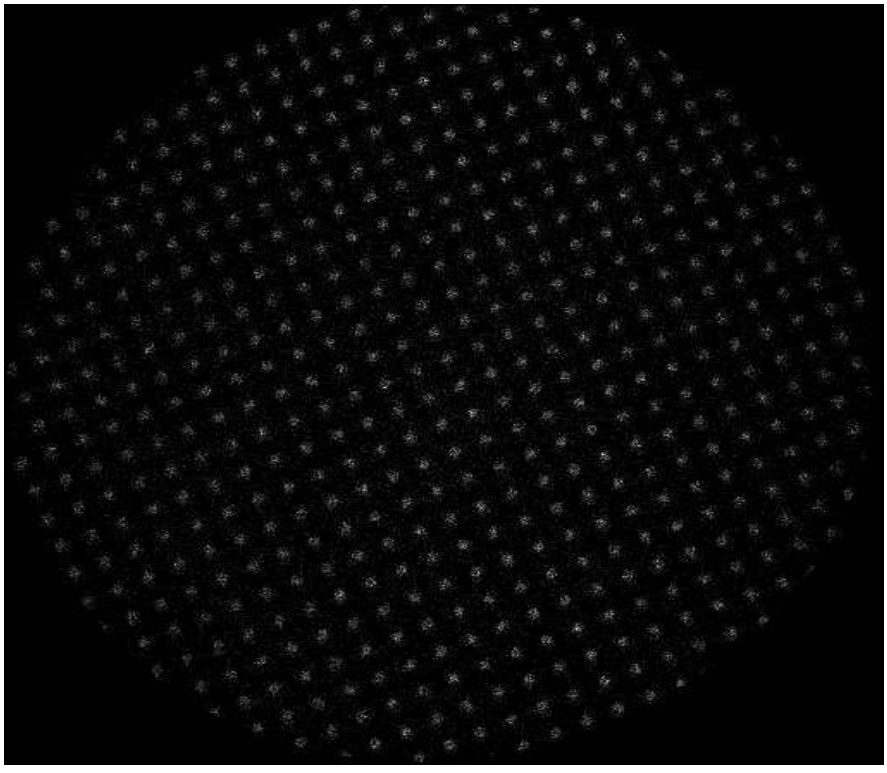

Figure 5. 4 Image in Photon Counting Mode (3S centroiding) [Stack of 3000 frames,Pin Hole Mask]

5.2 More Tests performed on UVIT EM DS:

1) Micro Channel Plate (MCP) voltage of HVU Vs Photon Counts. In that MCP voltage varied from 2020V to 1750V in step of 50V.
2) Interface test of EU with ISRO EM DHU (Data Handling Unit). In that imaging data has been taken through EM DHU instead of EGSE DHU. Electrically this test was successful, DHU team has taken all the clock, request and data timing waveforms from both channel (Main and Redt) and the results are as satisfactory. A detail report on this test will be prepared by ISRO DHU team.

Figure 5. 5 ISRO EM-DHU and UVIT EM-EU interface Test Setup

3) Bit error rate tests done by checking the parity bit in Photon Counting mode data only through CCDLAB software (new version) on science data received from EGSE and ISRO EM DHU. It was found that the bit error rate is of the order 10e-4 and not acceptable on the wired link. It was discussed with CSA and noted that they have not checked this at their end. So, current understanding is that the parity error detected was attributed to FPGA code timing problem. Even in Integration mode science data, algorithm of CRC word also not yet implemented inside EU and included in every 2Kbyte packet to validate correctness of data.

6. Bugs Occurred in EGSE during tests:

6.1 Failure of RAM slot in EGSE-DHU computer:

While doing interface test with ISRO EM DHU, it was found that DHU computer was not booting and this was told to CSA (Routes) to fix it. As per the guidelines sent by Mr. Joe, we tried to fix the bug. It was suspected that the EGSE DHU computer hard disk corrupted and it was diagnosed that the hard disk is working fine. Then RAMs on EGSE DHU computer checked and found that DDR4 slot of EGSE DHU computer was not

working. RAM from DDR4 slot removed and EGSE DHU computer booted properly. Imaging done with UVIT EM DS and science data recorded on EGSE DHU computer.

6.2 Communication Failure between EGSE BMU and EGSE DHU while Imaging:

After completing EM-EU and ISRO EM DHU test, EU is connected with EGSE DHU and there a bug was observed that communication between EGSE BMU and EGSE DHU fails while doing imaging. It has been told to CSA (Routes) to fix this bug. Some of the options has been tried to fix this bug as per CSA guidelines but the bug not yet fixed. We are still working to fix this bug.

This bug is fixed after changing the settings of DHU computer configuration file. This problem occurred because of changing RAM capacity from 4GB to 3GB (as per Routes inputs). Final fix to the communication problem needed a 'new code' sent by Routes (for specific 75% RAM). On one occasion (# as mentioned in # 6.1), the 'old' code did work even in this 75% RAM configuration. Routes believe that 'new code' is necessary to make any communication in this (75%) configuration.

7. Format of Science Data and its Storage

Science data output from EU is in format of 2K bytes packet in both Integration and Photon Counting imaging modes. The data details can be obtained from Doc: UVIT-911-00001-IDD02 [Science Data Interface Data Document]. First data gets stored in EGSE DHU computer. There is a separate hot swappable hard disk in EGSE DHU computer for science data storage. From that data can be taken out through portable 500GB USB hard disks as when required. For permanent storage of data, arrangements are being made. For carrying our planned four EM Ground Calibration Tests (Relative focus shift measurement, Detector Spectral calibration. Detector spatial sensitivity and Detector geometrical distortion) the space required for raw data storage is about 100 GB. Including the space required for processing a storage capacity of 400 GB is envisaged.

8. Software in Use for Data Analysis

The data from EU both in integration and photon counting modes can be inspected and even analyzed using the CCDLAB software developed by Joe Postma (Calgary University). CCDLAB is being installed both in IIA and CREST campuses. Some analysis is also being done using IRAF (Image Reduction and Analysis Facility). For analysis using IRAF, the raw format from EU are converted to FITS (Flexible Image Transport System) format using CCDLAB.

9. Result and Conclusion:

9.1 Micro Channel Plate (MCP) voltage of HVU Vs Photon Counts:

An experiment was undertaken to better understand the number of photons detected as a function of MCP voltage. A 515 pin hole mask was mounted, and six sets of images, with each set consisting of 3000 frames (in integration) mode were acquired, having MCP voltages between 2020 and 1720 volts in decreasing steps of 50 volts. One set of 3000 frames was also acquired at a MCP voltage of 1470 volts. This set of 3000 frames

were averaged and used as a master bias frames for further processing (in IRAF) of the image frames taken at MCP voltages between 2020 and 1720 volts. After the initial processing, we finally arrived at a set of 6 image frames (each set an average of 3000 frames) for MCP voltages of 2020, 1970,1920,1870,1820,1770 and 1720 volts respectively. The final image frame at 2020 volts is shown in Fig. 9.1.1. The pinholes are clearly seen in this image. The number of photons (within an aperture radius of 3 pixels) were estimated for each of the 6 final frames. As expected the detection of photons falls with decreasing MCP voltage. This is clearly seen in the graph shown in Fig. 9.1.2.

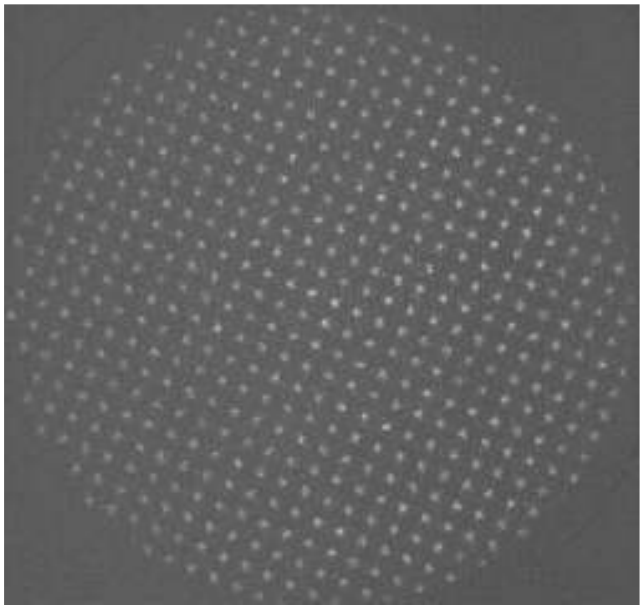

Figure 9.1. 1: An average of 3000 frames at 2020 V

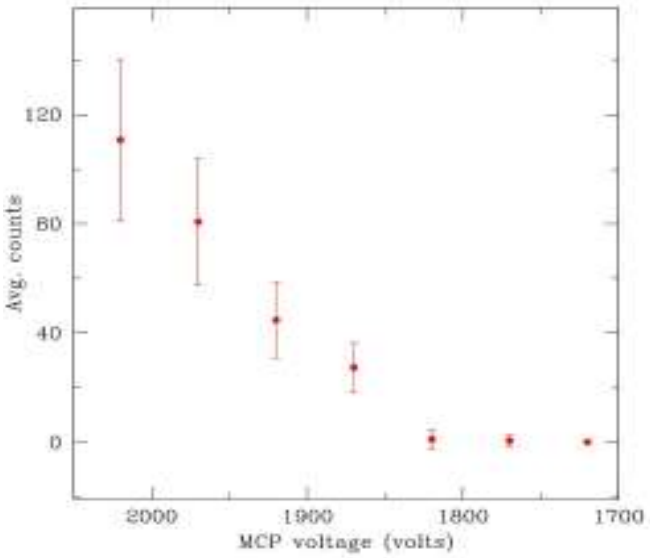

Figure 9.1. 2: Average number of detected counts against MCP voltage

The EM UVIT DS test at MGKM Lab was successful. By this test, it was learned, how to operate and handle the EM UVIT DS. During testing a couple of bugs occurred and also fixed, which gave the picture of handling such types of bugs, if it occurs again. Interface testing of EM-EU with EM-DHU cleared the test and complied with the design requirements. In EM-EU and EM-DHU test, the Parity check test on Science Data was not qualified. By this test, we came to know that, there is error in EU itself in generating the parity bits in the science data. This Parity check test on Science Data will be repeated with FM-EU and FM/ EM-DHU.