Implementation of 4K x 4K CCD Camera system for DFM Telescope
Introduction:

- This project (Mosaic 4K X4K CCD Camera system) has been initiated by Prof. A.K Pati, for use as imager in the 1.3M DFM Telescope to be installed at VBO, Kavalur.

- The team comprises of

1. Dr. R. Srinivasan
2. Anupama.K
3. P. Anbhazghan
4. Somashekar.M.R
5. Sagayanathan
CCD 4K*2K Characteristics

- Device : CCD 44-82 (2K*4K) from EEV Ltd.
- Format : 2048*4096
- Pixel Size : 15 μm Square
- Imaging Area : 30.7 * 61.4 mm
- Sensitivity: Back Illuminated, 84.2% QE @500 nm
- Three Side Buttable
- Full Well : 200 Ke/ Pixel
- Pixel readout frequency : 40 KHZ
- Grade : Scientific Grade 0
Butting CCDs

4k * 2k CCD  4k * 2k CCD  4k * 2k CCD

THE BUTTED
4K * 4K MOSAIC CCD
Mosaiced 4K X 4K CCD Camera System

- Any one CCD or Both can be selected
- Downloading DSP code
- Set Bias and clock voltages
- Initializes required memory
- Interleaved data scrambling with memory pointers
Hardware Details:

- DSP CPU Board
- Bias and Clocks Boards
- Analog Signal Processing Board
- Pre- amplifier Board
- Host interface Board
IIA CCD Architecture

- CCD Dewar
- Timing Generation
- Pipelining Data
- Thermal / Shutter Control
- Data Acquisition
  - User Interface
  - Image Display
  - Data Storage
  - Diagnostics
- CCD Controller
  - Sig. Proc.
  - A/D
  - Bias & clocks
  - DSP CPU
  - RS 422
- Host Environment
  - Data
  - SCI
  - RS 422
  - FIFO
  - Host I/F
  - Pentium PC
  - DAS
  - O S
CCD Dewar
DSP CPU Board

- Serial Bootstrap Loader (From Host)
- OnCE Port
- Thermal & Shutter Control
- Reset Mode Logic (Mode - 5)
- M 56002
  - 40 M Hz
  - P:512X24
  - X:256X24
  - Y:256X24
- Data 8 Bits
- D15 – D0
- Wait State Generator (D23 – D16)
- SCI
  - RS 422
  - Strobe
  - Sclk
  - Rx
  - Tx
- Bootstrap Loader (From Host)
The DSP CPU Board

- To receive and execute the program from the host
- To load all the DACs in the bias and clock boards
- To send the digitized data to the host with a strobe signal
- To generate the timing signals for readout of CCD
- Generation of hand shaking signals with the host computer
Bias and Clock Board

Bias Voltages (6)

Signal Processing
(5 Bits)

Backplane

Bias and Clock Board

12 Bit DAC
16 Bit Latches Timing

Board Addr. Decoder

12 Bit DAC

A

A

A

11 Clocks

L1,L2,L3
L4,L5
P1,P2,P3
P4,P5
Reset

Sig/Ref
Int.Reset
Int.Hold
ADC
Convert

VDD
VRD
VGMOS
VSA
PROT

Filter

BUF

12 Bit DAC

12 Bit DAC
The key feature of any control system is timing.

Numerous events must occur in strict time order and at precise time intervals.

Thus the bias and the Clocks board configure all the necessary bias and clock voltages and timing activities required for CCD.
Analog Signal Processing board

Functional block diagram of Analog Processing Board
Analog Signal Processing Board

- DC offset removal
- Pre-amplification
- Double correlated sampling
- Bias offset and Digitization of the signal
Host interface card

- 16-bit Data Buffers
- 8/16 I/F
- Addr, Decode
- 8K FIFO 16-bit
- Baud Rate Gen.
- 16-bit UART
- Rs 422 Tx/Rx
- Rs 422 (Rx)
- FIFO Status Reg.
- 8K FIFO 16-bit
- Data
- Strobe
- Host interface card

Diagram shows connections and flow of data and signals between components.
Host Interface Card

- Asynchronous serial communication
- USART-8251
- FIFO
- Bootstrap loading
- Digitized data on parallel port
Hardware Layout for Mosaiced CCD

- **Bias & Clocks Board #2**
  - D15-D0
  - Clocks
  - Biases
  - To CCD #2

- **Analog Processing Board**
  - 8 bit data
  - 5 Sig.Proc. Controls, 8 ADC data selects
  - D15-D0

- **Bias & Clocks Board**
  - 8 biases, 2 ADC offsets, 11 clocks, 5 analog signal processing control bits
  - 8 ADC data Selects
  - D15-D0

- **DSP 56002 – 40M Hz**
  - Wait state delay counter
  - Commands on SCI
  - Data – RS422 (8 bits)
  - D15-D0

- **Host Computer**
  - SCI
  - ISA - I/F
  - Data RS422

- **CCD O/P**
  - To CCD #1
Current Status

- Dewar fabrication is completed in our mechanical workshop to accommodate a 4K*4K system by Mr. Sagayanathan.

- Dewar is vacuum tested and LN2 holding time is presently 24 Hrs.

- 90mm Shutter has been ordered with M/s Vincent Associates.

- CCD controller unit has been built to hold the 4 PCBs.

- The Software configuration and Testing is in progress.

Configuring the CCD controller

- Start
- Load DSP code
- Load bias and Clock voltages
- Enable bias
- Reset ADC
- Send parameters
- Allocate memory
- Display 'Controller ready'
Acquire a Frame

1. Preflush
2. Expose
3. Reset FIFOs
4. Read the frame
5. Display the acquired image
Programming in DELPHI under Windows

- Provides GUI capability
- Large memory access
- Event driven architecture
- Reusable code
SPECTRAL RESPONSE OF CCD (02453-05-01)

QE(%) vs. nm

0 400 500 600 700 800 900 1000

300 400 500 600 700 800 900 1000

nm

QE(%)
SPECTRAL RESPONSE OF CCD (02453-06-01)
Programming bias and clock voltages

- Setting bias voltages

- Setting clock voltages
THANK YOU