Implementation of 4K x 4K CCD Camera system

for

DFM Telescope

Introduction:

- This project (Mosaic 4K X4K CCD Camera system) has been initiated by Prof.A.K Pati ,for use as imager in the 1.3M DFM Telescope to be installed at VBO, Kavalur.

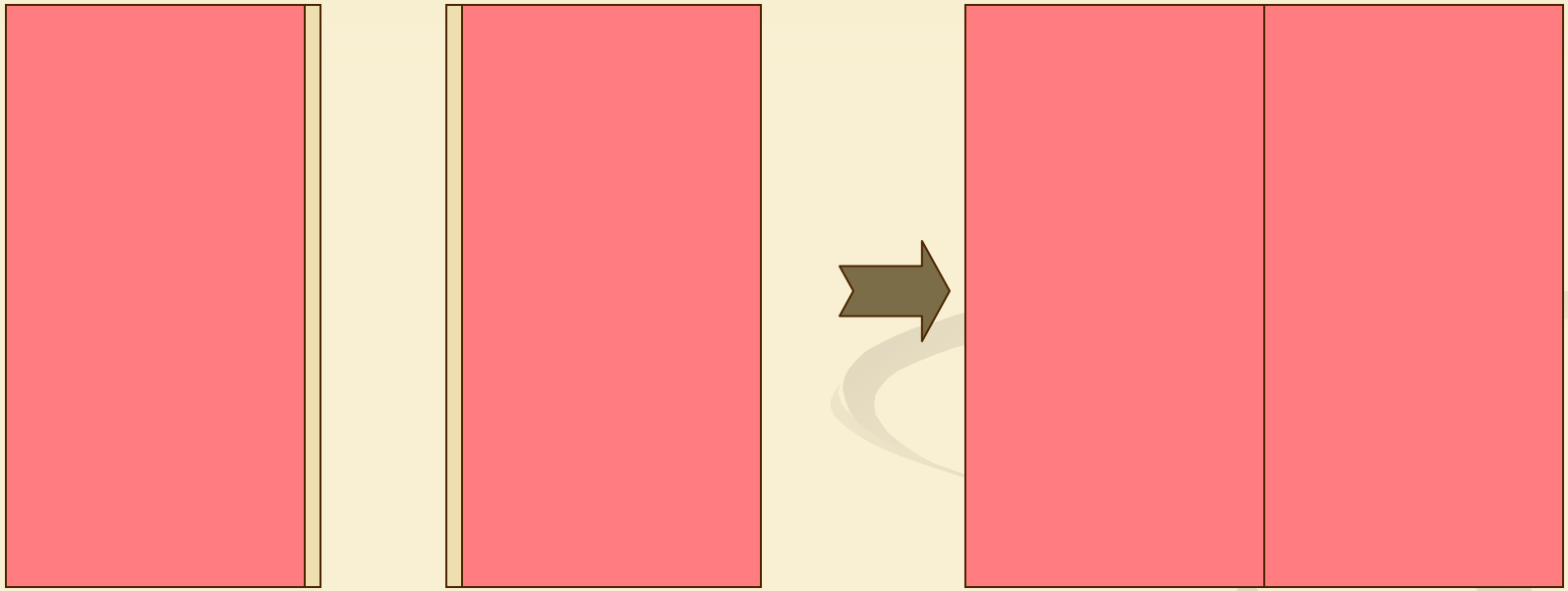
- The team comprises of

1. Dr.R.Srinivasan
2. Anupama.K
3. P.Anbhazghan
4. Somashekar.M.R
5. Sagayanathan

CCD 4K*2K Characteristics

- Device : CCD 44-82 (2K*4K) from EEV Ltd.
- Format : 2048*4096
- Pixel Size : 15 µm Square
- Imaging Area : 30.7 * 61.4 mm
- Sensitivity: Back Illuminated, 84.2% QE @500 nm
- Three Side Buttable
- Full Well : 200 Ke/Pixel
- Pixel readout frequency : 40 KHZ
- Grade : Scientific Grade 0

Butting CCDs



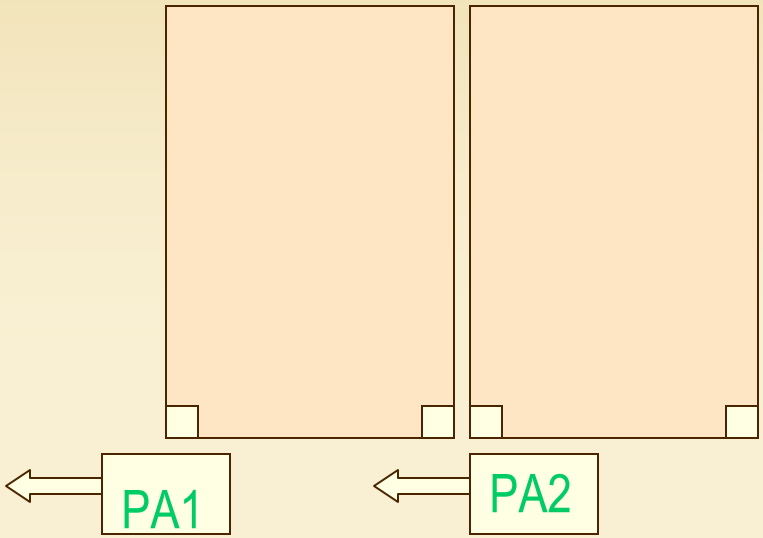
4k * 2k CCD

4k * 2k CCD

THE BUTTED

4K * 4K MOSAIC CCD

Mosaiced 4K X 4K CCD Camera System

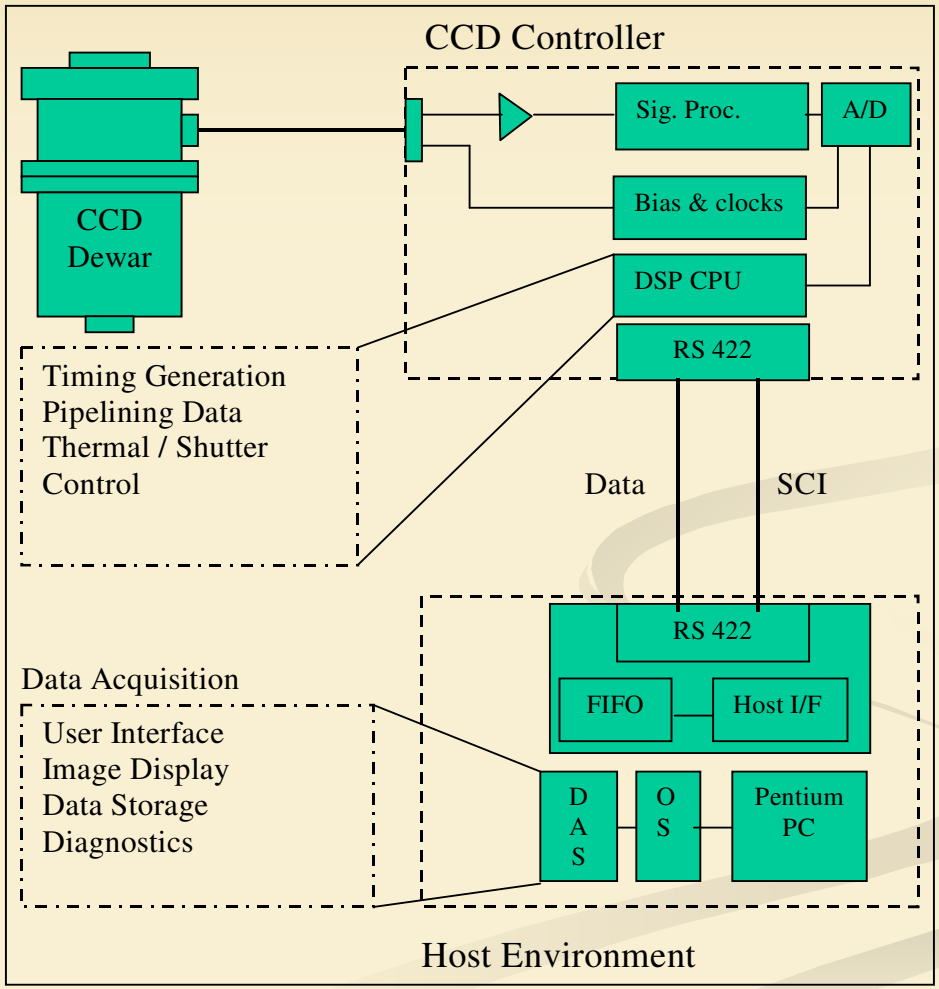


- Any one CCD or Both can be selected
- Downloading DSP code
- Set Bias and clock voltages
- Initializes required memory
- Interleaved data scrambling with memory pointers

Hardware Details:

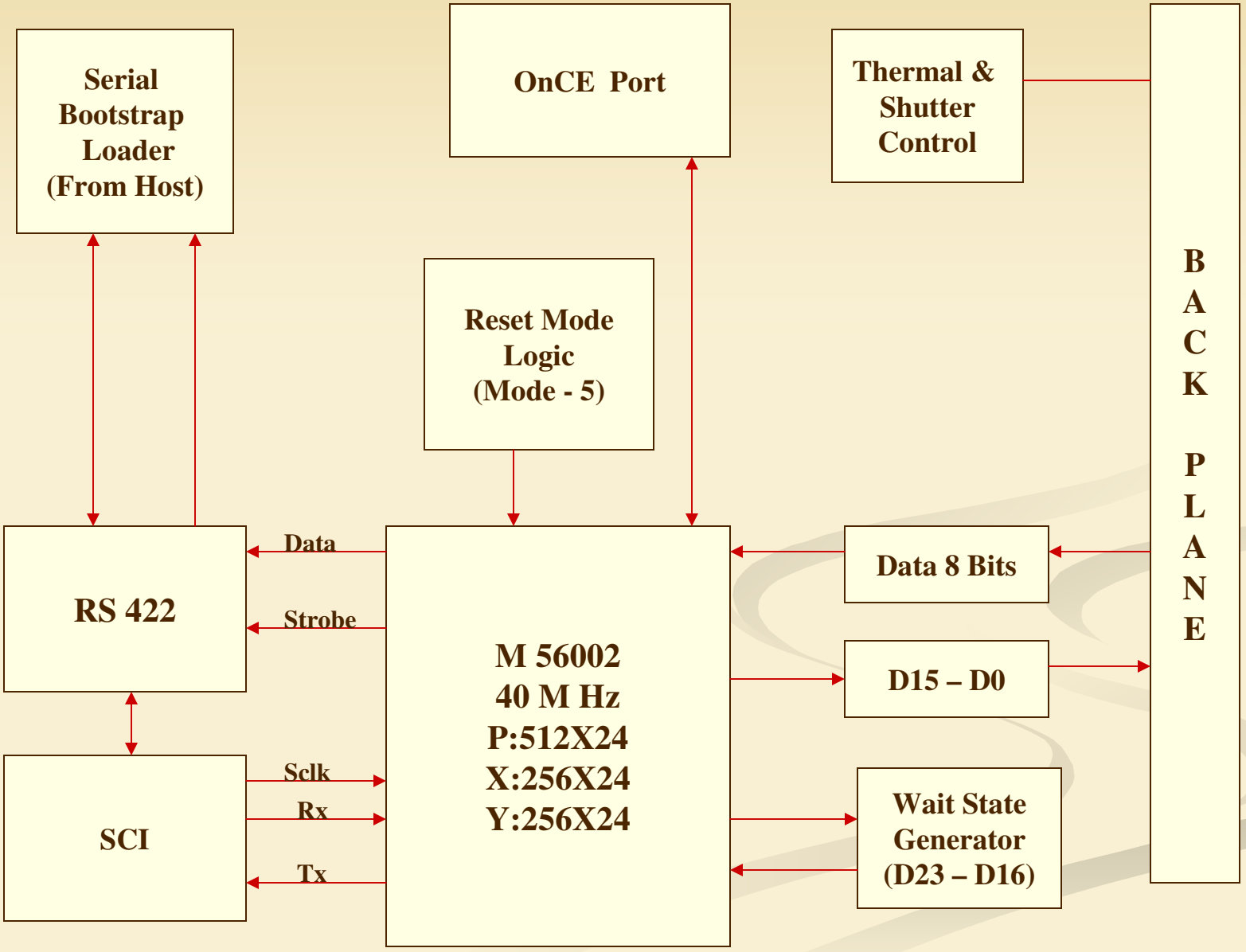
- DSP CPU Board
- Bias and Clocks Boards
- Analog Signal Processing Board
- Pre - amplifier Board
- Host interface Board

IIA CCD Architecture



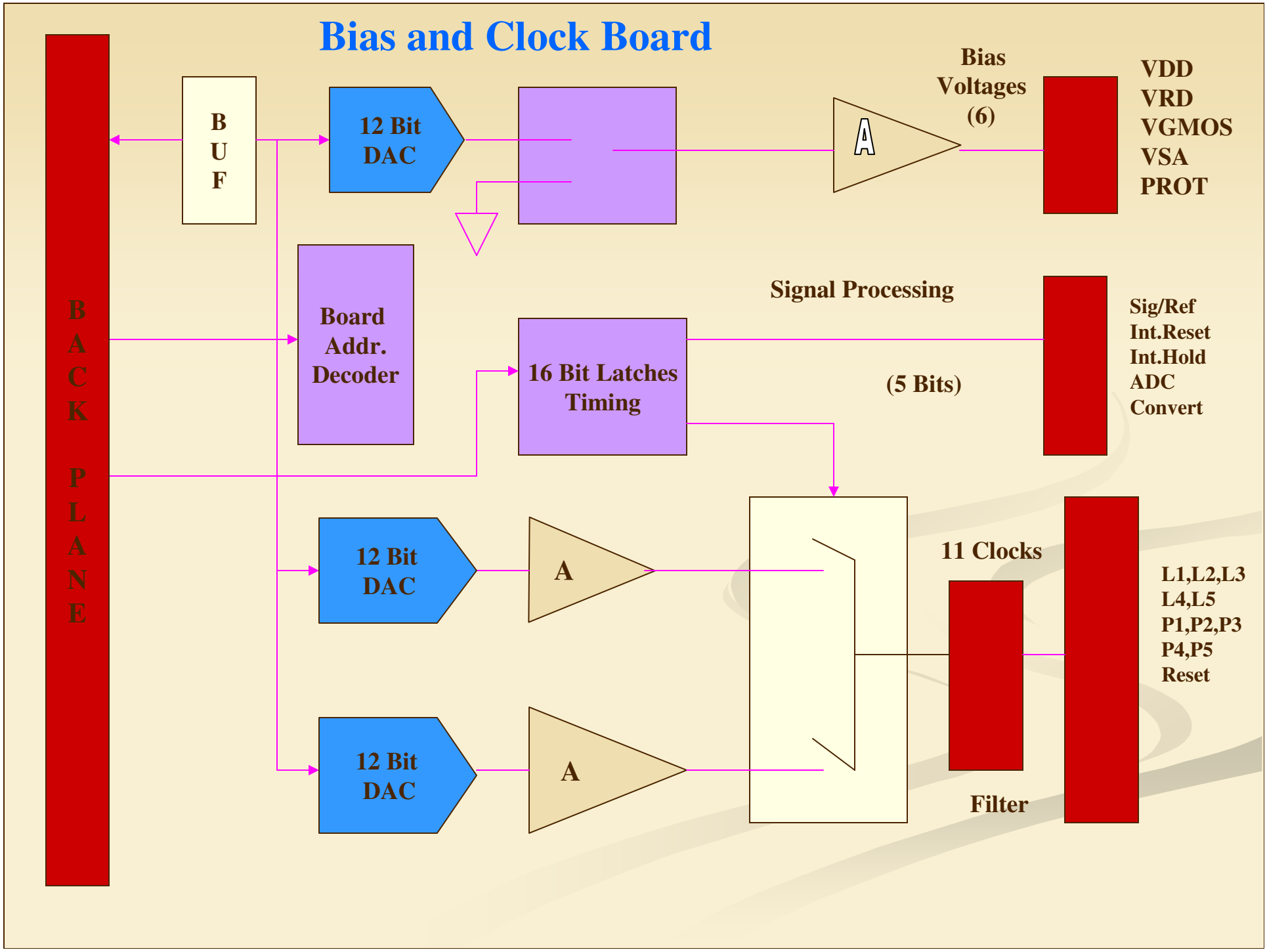
CCD Dewar

DSP CPU Board



The DSP CPU Board

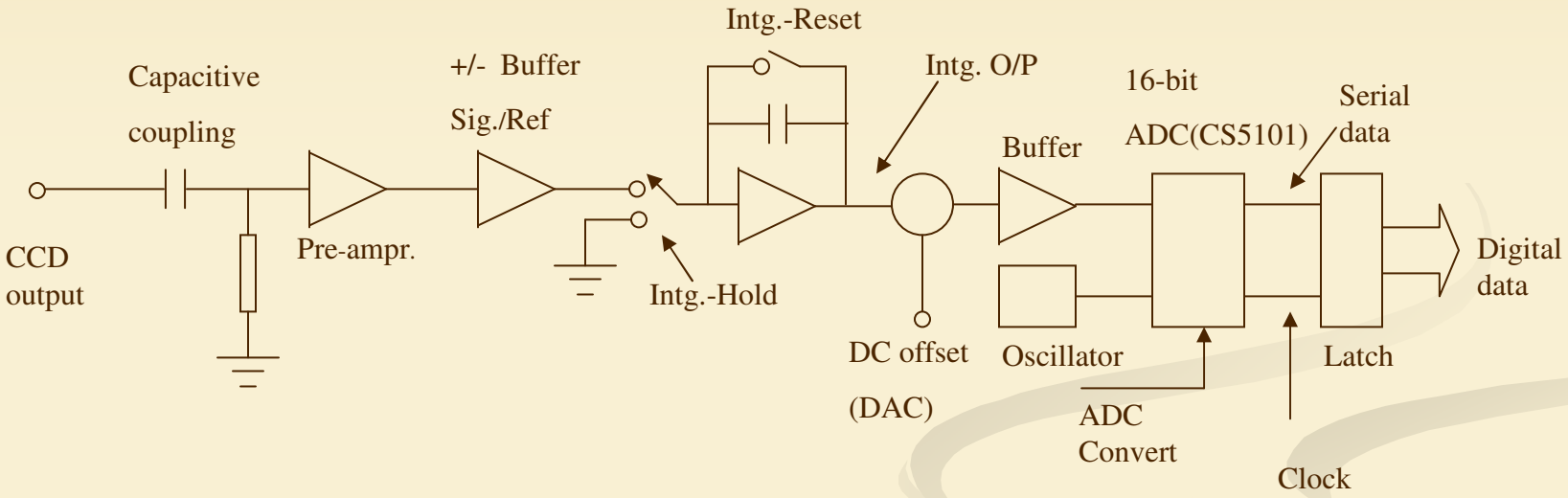
- To receive and execute the program from the host
- To load all the DACs in the bias and clock boards
- To send the digitized data to the host with a strobe signal
- To generate the timing signals for readout of CCD
- Generation of hand shaking signals with the host computer


Bias and Clock Board
BACK PLANE
BUF
12 Bit DAC
A
Bias Voltages (6)
VDD
VRD
VGMOS
VSA
PROT
Board Addr. Decoder
16 Bit Latches Timing
Signal Processing
(5 Bits)
Sig/Ref
Int.Reset
Int.Hold
ADC Convert
12 Bit DAC
A
12 Bit DAC
A
11 Clocks
Filter
L1,L2,L3
L4,L5
P1,P2,P3
P4,P5
Reset

Bias and Clock Board

- The key feature of any control system is timing.
- Numerous events must occur in strict time order and at precise time intervals.
- Thus the bias and the Clocks board configure all the necessary bias and clock voltages and timing activities required for CCD.

Analog Signal Processing board

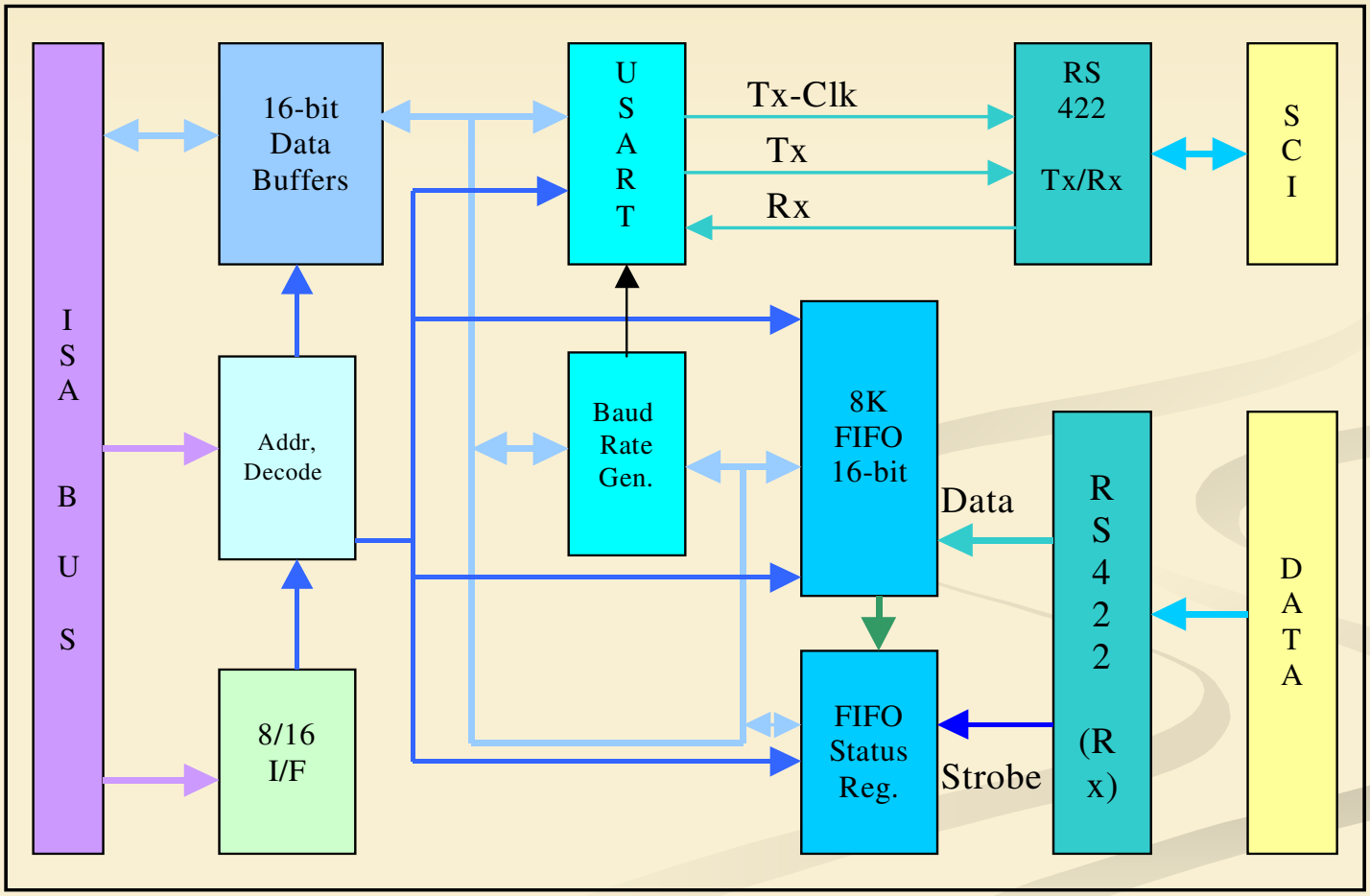


Functional block diagram of Analog Processing Board

Analog Signal Processing Board

- DC offset removal
- Pre-amplification
- Double correlated sampling
- Bias offset and Digitization of the signal

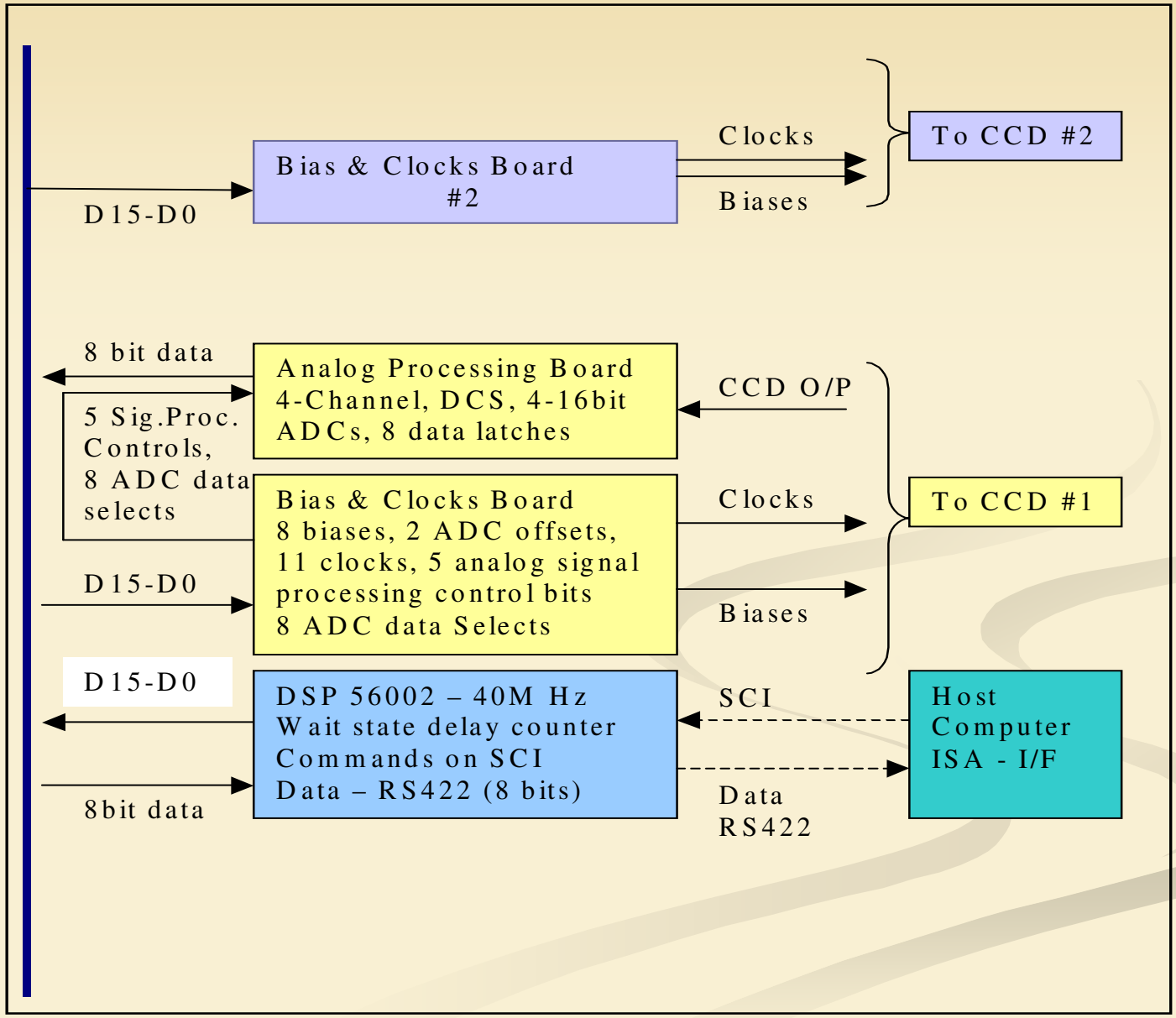
Host interface card



Host Interface Card

- Asynchronous serial communication
- USART-8251
- FIFO
- Bootstrap loading
- Digitized data on parallel port

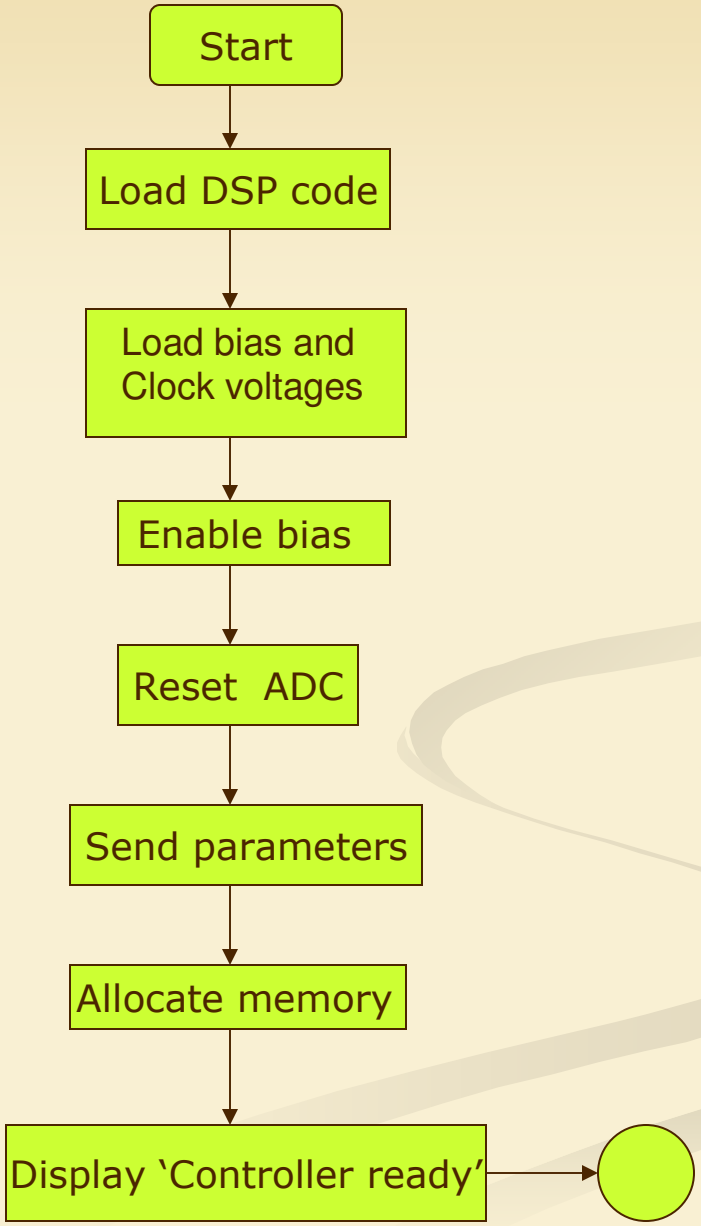
Hardware Layout for Mosaiced CCD



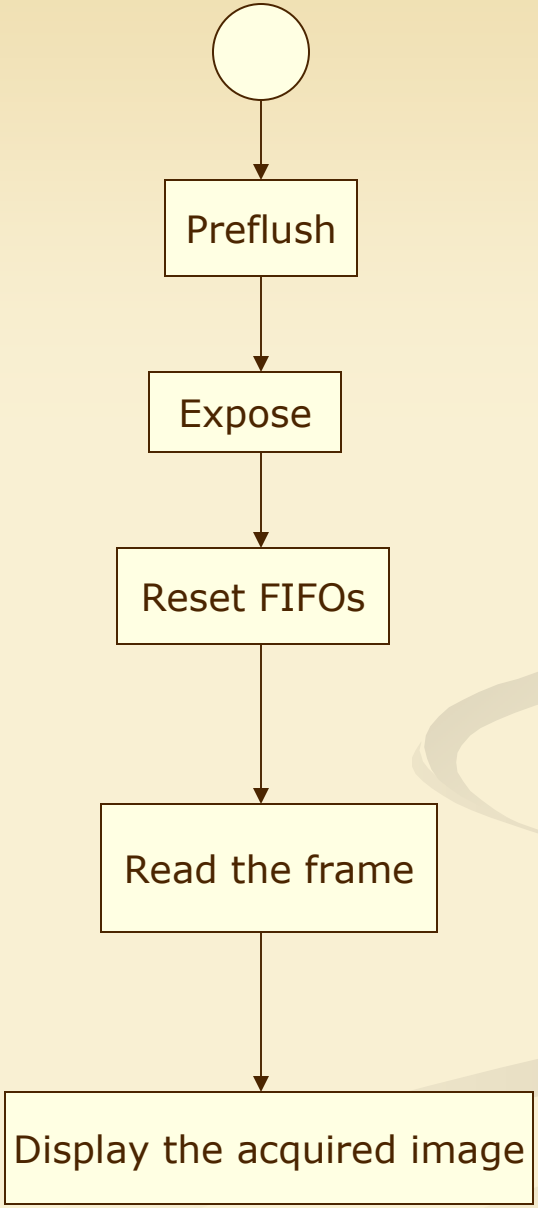
Current Status

- Dewar fabrication is completed in our mechanical workshop to accommodate a 4K*4K system by Mr.Sagayanathan.
- Dewar is vacuum tested and LN2 holding time is presently 24 Hrs.
- 90mm Shutter has been ordered with M/s Vincent Associates.
- CCD controller unit has been built to hold the 4 PCBs.
- The Software configuration and Testing is in progress.
- Anticipated Completion : March 2008.

Configuring the CCD controller



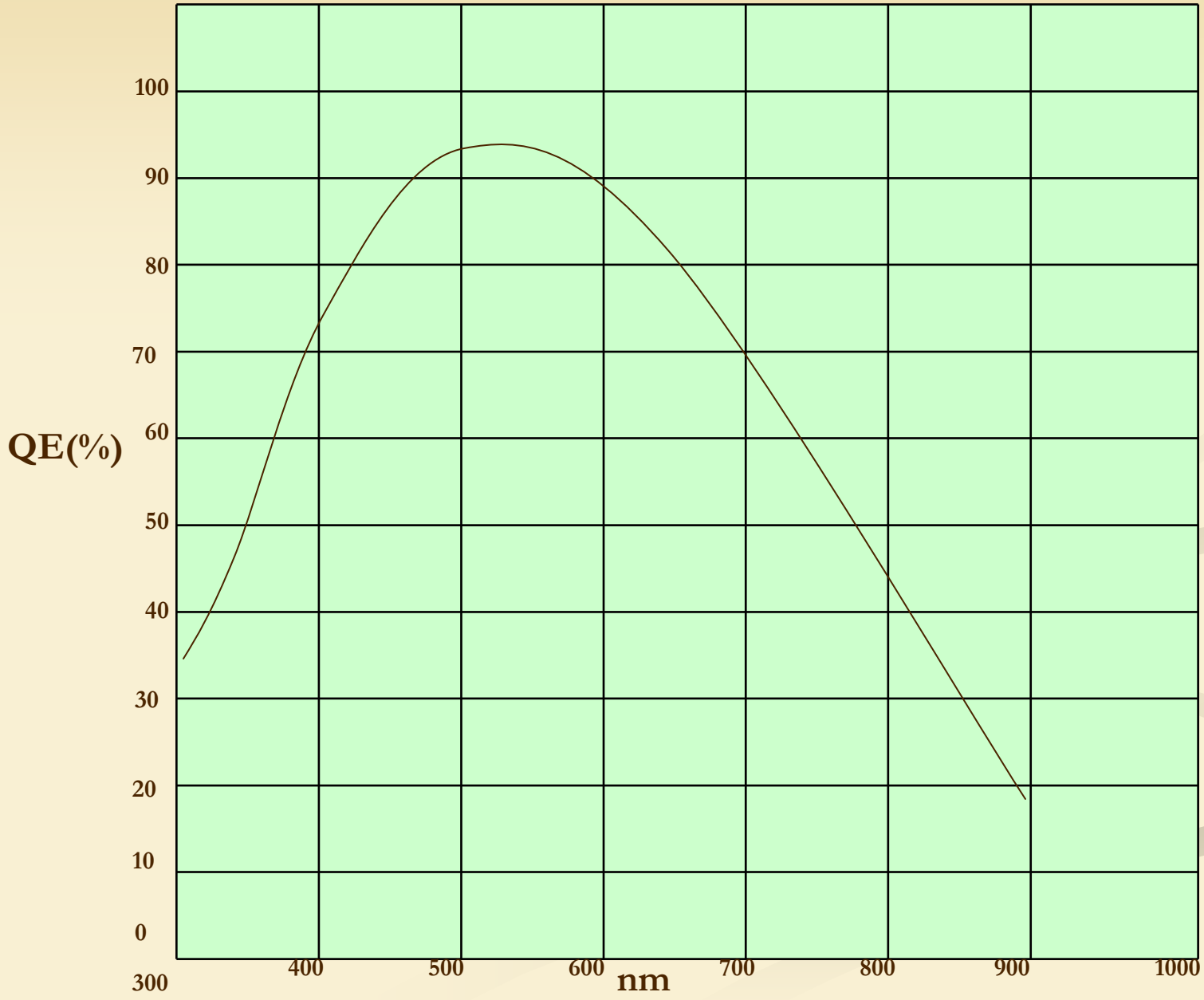
Acquire a Frame



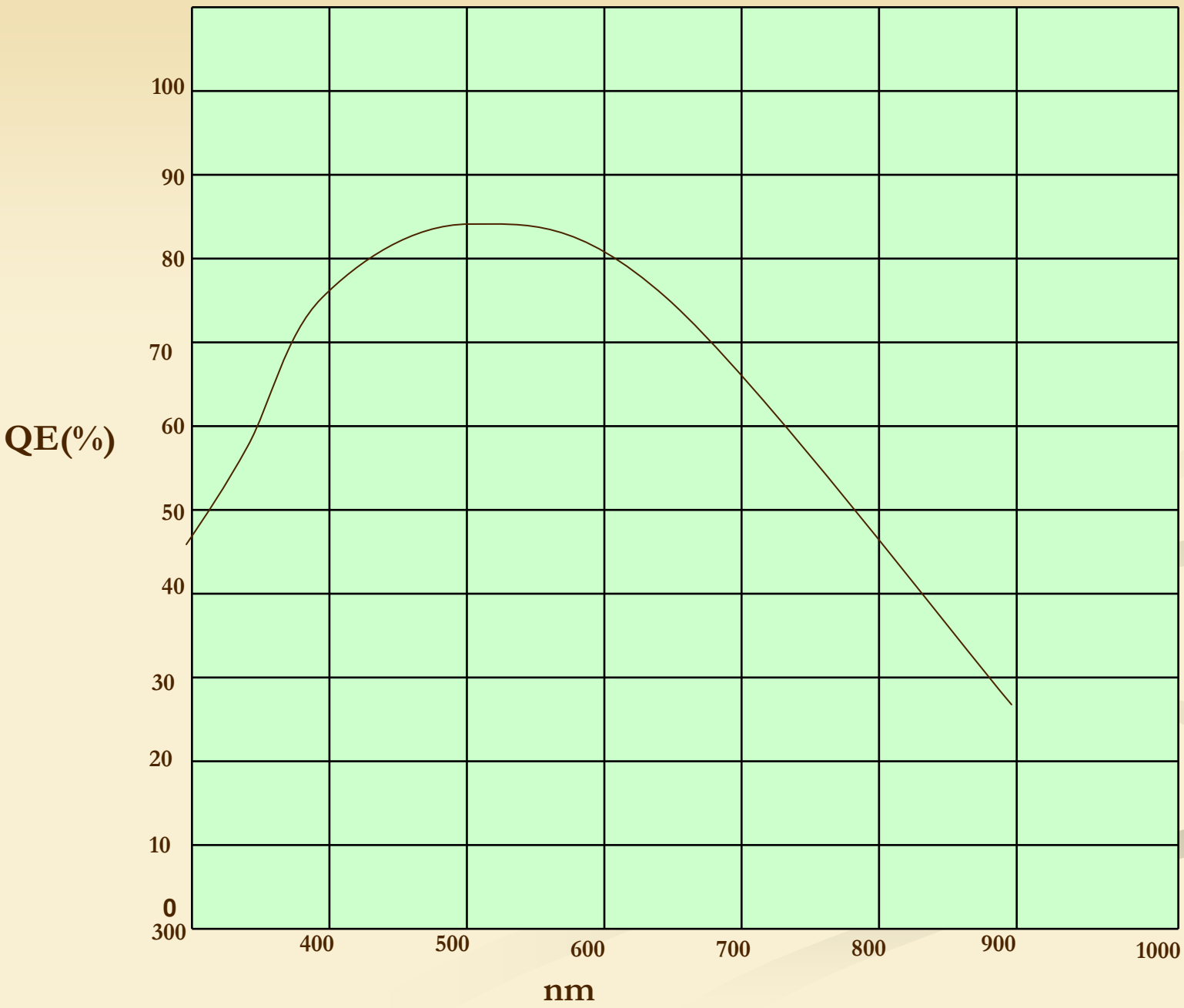
Programming in DELPHI under Windows

- Provides GUI capability
- Large memory access
- Event driven architecture
- Reusable code

SPECTRAL RESPONSE OF CCD (02453-05-01)



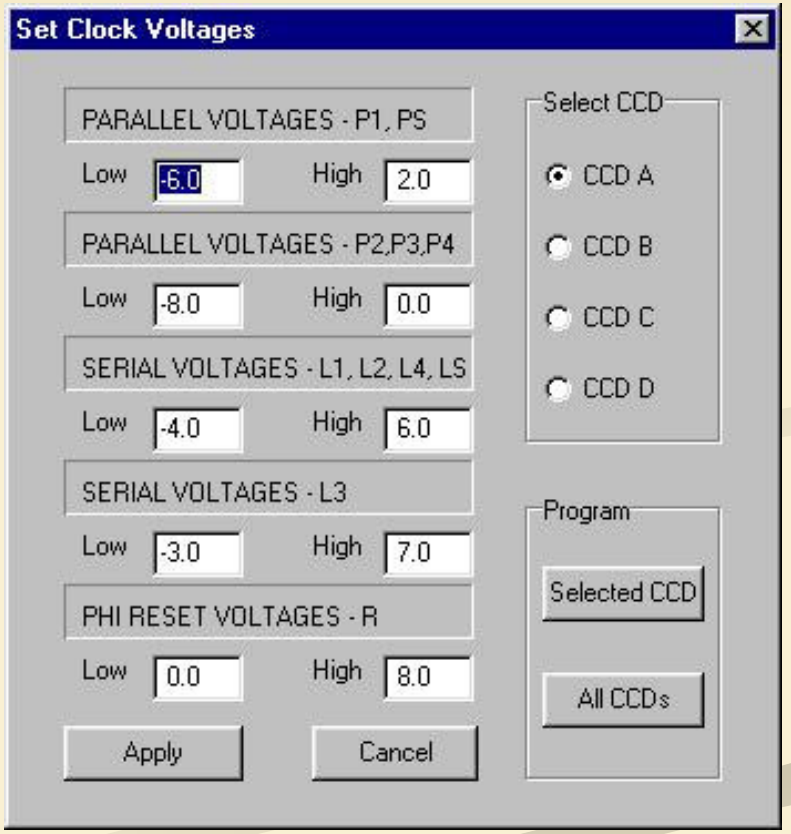
SPECTRAL RESPONSE OF CCD (02453-06-01)



Programming bias and clock voltages

- Setting bias voltages

- Setting clock voltages



THANK YOU